II. Remarks

Reconsideration and re-examination of this application in view of the above amendments and the following remarks is herein respectfully requested.

After entering this amendment, claims 5-9, 25, and 26 remain pending.

Claim Rejections - 35 U.S.C. §103

Claims 9 and 5-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. 2003/0107052 A1 to Chan et al. in view of U.S. Patent No. 5,908,313 to Chau et al. (Chau).

Chan not only fails to disclose the "seed layer" but in particular does not teach or suggest a "widening of the source and drain depressions, in an upper region, with a predetermined depth" and which is filled by a "filling layer."

In the present application, a well defined "channel" is realized by etching away the spacer 7 which results in a "widening with a predetermined depth d1" at the surface of the depression or recess V1. This depression including now a well defined "**step**" is filled with an electrically **conductive filling material** 13. Thus, according to the present application the "channel length" is defined very precisely by the widening filled with filling material, i.e. the etch process defines the widening of the recess V1. Moreover, since the widening is filled by a filling material (and not by doping or implantation) extremely steep doping profiles can be realized between the channel region and the source/drain regions.

In contrast, Chan discloses an epi-Si layer 118 on top of the source and drain regions which are already filled with an epi layer 116. Thus, there exists no physical

widening with a predetermined depth at the surface of the depressions. The regions 116, which may be compared to the channel connection regions of the present application, are merely realized by ion implantation 134 and thermal treatment within the same epi layer 118. Moreover, according to Chan the channel connection regions have a smaller width than the filled source and drain regions 116.

In particular, Chan neither discloses nor suggests precisely defining the channel dimensions of a FET by a recess or widening in its upper portion which is filled by a material different from the material of the channel. Thus, an improvement of the electrical characteristics of a transistor as realized in the present application cannot be achieved by the transistor structure according to document Chan.

Moreover, Chau merely discloses to use a seed layer for the filling layer. However, Chau it is silent with respect to the "widening with a predetermined depth" or "step shaped portion" at the surface of the depression, which is filled by a material different from the material of the channel region.

New Claims 25 and 26

Claims 25 and 26 depend from claim 9 and are, therefore, patentable for at least the same reasons as given above in support of claim 9.

In addition, new claim 25 more specifically defines that a step is formed in the source and drain depressions at the widening. Further, new claim 26 also defines that the material filling the widening is different from the material of the seed layer.

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that the present form of the claims are patentably distinguishable over the art of record and that this application is now in condition for allowance. Such action is requested.

Respectfully submitted by,

Dated: November 12, 2008

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